Certificate

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[Title of the Invention] Coded and Multiplexed Signal Reproduction Apparatus

[Claims]

[Claim 1] A coded and multiplexed signal reproduction apparatus comprising:

a first multiplexed signal analysis unit for detecting a desired code sequence from code sequences in which data are multiplexed by using a synchronous signal and a packet length;

a second multiplexed signal analysis unit for analyzing codes after the synchronous signal detected by the first multiplexed signal analysis unit, on the basis of synchronous signal establishment information generated by the first multiplexed signal analysis unit;

a data separation control unit for recognizing the boundary of packets on the basis of synchronization establishment information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit; and

a formatter unit for generating data according to packet boundary information based on the synchronization establishment information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit, and inserting the data sequence in a predetermined position of separated data.

[Claim 2] A coded and multiplexed signal reproduction apparatus as a multiplexed video signal separation apparatus for

separating a data sequence multiplexed by using a synchronous signal, a packet length, and packet header information including data reproduction information, comprising:

a multiplexed signal analysis unit for analyzing a packet header;

a data separation unit for performing desired data separation on the basis of the analysis result from the multiplexed signal analysis unit; and

a formatter unit for inserting reproduction information obtained in the multiplexed signal analysis unit in a predetermined position of the separated data.

[Claim 3] A coded and multiplexed signal reproduction apparatus as an image signal reproduction apparatus comprising a coded and multiplexed signal separation unit having a pipeline structure and an image signal decoding unit, wherein:

when detecting a code sequence indicating the end of multiplexed data, the multiplexed signal separation unit adds padding data to the rear of the code sequence indicating the end of the multiplexed data.

[Claim 4] A coded and multiplexed signal reproduction apparatus having a pipeline structure wherein, when a signal of a specific data sequence is input, it is recognized as an input end of multiplexed data, and the pipeline is cleared.

[Detailed Description of the Invention]

[0001]

[Applicable Field in Industry]

The present invention relates to a coded and multiplexed signal reproduction apparatus and, more particularly, to improvement of an apparatus which performs reproduction of a digital code sequence in which audio, video, and other additional information are multiplexed, such as video CD, DVD, and digital CS broadcasting.

[0002]

In recent years, media for recording and transmitting digital-coded and multiplexed video signal, audio signal, and additional information signal such as subtitle information, have spread rapidly, like video CD, DVD, and digital CS broadcasting. However, in order to spread apparatuses for reproducing the above-described coded and multiplexed digital signals for domestic use or the like, cost down of the reproduction apparatuses is indispensable. For this purpose, it is required to implement a demultiplexer for demultiplexing the multiplexed signal and a decoder for decoding the demultiplexed digital signals, with simple and compact circuit constructions.

[0003]

By the way, in such digital media, a coding method defined by MPEG standard is generally used for video signals. On the other hand, for audio signals, coding methods other than the MPEG coding method are adopted in many cases. For multiplexing coded data of video and audio, a multiplexing method defined by the

standard of the MPEG system is adopted.

[0004]

Figure 3 shows examples of coded data of video information, audio information, and additional information which are multiplexed by using packets. The multiplexed and coded data are subjected to byte alignment. An audio signal and a video signal are respectively digital-coded by an encoder and then multiplexed in packet units by a multiplexer. At the head of each packet, a packet header H is attached, which is composed of a synchronous signal S indicating the packet head (hereinafter, referred to as a packet start code prefix code), an identifier I for identifying the packet as one of an audio packet, a video packet, and an additional information packet, packet length information L indicating the length of the packet, video and audio synchronous reproduction information R, and the like. After the packet header H, according to the type of the packet, one of coded data CDP of the video signal, coded data CDS of the audio signal, and coded data CDA of the additional information is placed.

[0005]

When coding a video signal, hierarchical coding is performed, for example, the video is divided into bands and coded, and a code sequence indicating the start of the hierarchy and a code sequence indicating the name of the hierarchy are used. The same code sequence is used for the code sequence indicating the start of the hierarchy and the above-mentioned start code prefix code

indicating the head of the packet.

[0006]

Usually, since the prefix code of the packet start code appears in the multiplexed data sequence for every data unit indicated by the packet length included in the packet header information, there occurs no mixing of the coded video data and the hierarchy start code.

[0007]

However, in a packet including coded video data, in contrast with a packet including coded audio data, there is a case where multiplexed data the packet length of which is undefined is input. This situation occurs, for example, in a multiplexed data sequence in which a transport packet used for digital CS broadcasting or the like is converted to a PES (Pakettaized Elementary Stream) packet. Hereinafter, a description will be given of the conventional manner of demultiplexing multiplexed data in the case where the packet length of coded video data is undefined.

[0008]

Figure 2 is a diagram illustrating an example of a conventional coded and multiplexed signal separation apparatus. In the figure, 2s1 denotes a coded and multiplexed signal supply unit which supplies a coded and multiplexed signal to this separation apparatus, and this corresponds to a part before a decoder of a player for a video CD or DVD or a digital CS tuner.

2s2 denotes an input buffer which receives the output from the coded and multiplexed signal supply unit 2s1, and this is constituted by, for example, a ring buffer. 2s4 denotes an input buffer reading control circuit which controls read addresses given to the input buffer 2s2 to perform reading control. SW1 denotes a switch which connects the output from the input buffer 2s2 with one of three terminals a, b and c. 2s3 denotes a start code prefix code detection unit which receives a signal when the switch SW1 is placed on the terminal b and detects a start code prefix code included in a packet, and this corresponds to a first multiplexed signal analysis unit which detects a desired code sequence from code sequences in which data are multiplexed, by using a synchronous signal and the packet length. Further, 2s5 denotes a start code discrimination unit which receives an output signal from the start code prefix code detection unit 2s3, and decides that the start code is included in one of the packets of video signal, audio signal, and additional information. 2s6 denotes a header analysis unit which analyzes a header on receipt of an output signal from the start code discrimination unit 2s5 and a signal from the input buffer 2s2 when discrimination of the start code is ended and the switch SW1 is placed at the terminal a, and this corresponds to a second multiplexed signal analysis unit which analyzes codes that follow the synchronous signal detected by the first multiplexed signal analysis unit on the basis of synchronous signal establishment information generated

by the first multiplexed signal analysis unit. 2s7 denotes a reproduction information hold unit which receives an output signal from the header analysis unit 2s6 and holds reproduction information. 2s8 denotes a data separation control unit which receives a signal from the input buffer 2s2 when the switches SW1 and SW2 are placed at the terminals c and f, respectively, and recognizes the boundary of packets to perform data separation control. 2s15 denotes an input buffer protection unit which controls the contents of the input buffer 2s2 to protect the contents when the start code prefix code detection unit 2s3 detects a prefix code. 2s16 denotes a start code status correction unit which makes the start code prefix code detection unit 2s3 correct the status of the start code in accordance with the result of the decision by the start code discrimination unit 2s5. 2s17 denotes a decoding buffer write pointer correction unit which performs correction of a write pointer to the decoding buffer 2s9 in accordance with the result of the decision by the start code discrimination unit 2s5. 2s18 denotes an input buffer read pointer correction unit which performs correction of an input buffer read pointer of the input buffer read control circuit 2s4 in accordance with the result of the decision by the start code discrimination unit 2s5. SW3 denotes a switch which selects one of the output from the start code prefix code detection unit 2s3 and the output from the terminal c of the switch SW1, and outputs the signal to the data separation control

unit 2s8. 2s19 denotes a controller which performs switching control of the switches SW1 and SW3.

[0009]

Further, 2s denotes a multiplexed signal separation unit comprising the above-mentioned switch SW1, switch SW3, start code prefix code detection unit 2s3, start code discrimination unit 2s5, header analysis unit 2s6, reproduction information hold unit 2s7, data separation control unit 2s8, input buffer protection unit 2s15, start code status correction unit 2s16, decoding buffer write pointer correction unit 2s17, and the input buffer read pointer correction unit 2s18.

[0010]

Further, 2s10 denotes a decoding unit which decodes the signal from the data separation control unit 2s8 by using the reproduction information held by the reproduction information hold unit 2s7. 2s9 denotes a decoding buffer which receives the output signal from the data separation control unit 2s8, holds this signal, and supplies this signal to the decoding unit 2s10. 2s11 denotes a work memory to be used when the decoding unit 2s10 performs decoding operation. 2s12 denotes a host CPU which performs processes such as initialization and reset of the decoding unit 2s10, and its host bus HB is connected with the reproduction information hold unit 2s7 and the decoding unit 2s10. Further, 2 denotes a coded and multiplexed signal reproduction apparatus comprising the above-mentioned constituents except the

coded and multiplexed signal supply unit 2s1, the host bus HB, the host CPU 2s12, and the controller 2s19, i.e., it comprises the input buffer 2s2, the input buffer reading control circuit 2s4, the switch SW1, the switch SW3, the start code prefix code detection unit 2s3, the start code discrimination unit 2s5, the header analysis unit 2s6, the reproduction information hold unit 2s7, the data separation control unit 2s8, the input buffer protection unit 2s15, the start code status correction unit 2s16, the decoding buffer write pointer correction unit 2s17, the input buffer read pointer correction unit 2s18, the decoding buffer 2s9, the decoding unit 2s10, and the work memory 2s11.

[0011]

Next, the operation will be described. A coded and multiplexed data sequence supplied from the coded and multiplexed signal supply unit 2s1 is once stored in the input buffer 2s2. Under control of the controller 2s19, initially, the switch SW1 is connected to the contact b. The multiplexed data sequence stored in the input buffer 2s2 is output byte by byte toward the start code prefix code detection unit 2s3, under control of the input buffer reading control circuit 2s4. The start code prefix code detection unit 2s3 detects a packet start code which is a head code of packetized data, and activates the start code discrimination unit 2s5. The start code discrimination unit 2s5 decides the type of the input packet by using that a video packet, an audio packet, and an additional information packet have

different packet identifiers. When the packet identifier which follows the start code prefix code is an identifier which indicates a desired data sequence to be reproduced, the start code discrimination unit 2s5 posts that the input packet is an effective packet, to the header analysis unit 2s6. Whether the packet is an effective packet or an ineffective packet, the start code discrimination unit 2s5 activates the header analysis unit 2s6.

[0012]

When the start code discrimination unit 2s5 decides that the input packet is an audio packet or an additional information packet, since analysis of the start code is not necessary, the start code discrimination unit 2s5 places the switch SW1 on the contact c and the switch SW2 on the contact f by using the controller 2s19, whereby the output packet from the input buffer 2s2 is directly output to the data separation control unit 2s8. The data separation control unit 2s8 controls data transfer of this audio packet or additional information packet to the decoding buffer 2s9.

[0013]

The decoding unit 2s10 decodes the audio packet or additional information packet stored in the decoding buffer 2s9, by using an internal audio decoder or additional information decoder, temporarily stores the decoded signal in the work memory 2s11, and reads the decoded signal from the work memory 2s11 to

output it to the outside as a reproduced signal.

[0014]

When the input packet is decided as a video packet according to the result of the decision by the start code discrimination unit 2s5, the controller 2s19 changes the position of the switch SW1 from the contact b to the contact a to output the video packet to the header analysis unit 2s6. The header analysis unit 2s6 receives the packet from the input buffer 2s2, analyzes the packet length and the reproduction information to be used for reproduction, which are included in the packet header, and stores the reproduction information in the reproduction information hold unit 2s7. Further, the header analysis unit 2s6 detects the end of the header in accordance with header information. While performing the processes on the video data, the controller 2s19 places the switch W3 at the contact g and activates the data separation control unit 2s8. The data separation control unit 2s8 controls data transfer to the decoding buffer 2s9, on the basis of data separation information possessed by the header analysis unit 2s6.

[0015]

The coded video data stored in the decoding buffer 2s9 is decoded by the video decoder in the decoding unit 2s10, like the coded data of audio and additional information, whereby a reproduced signal is output. The decoding unit 2s10 performs the decoding process by using the work memory 2s11. At this time, it

performs the decoding operation so that the coded video data is synchronized with the coded audio data, by using the reproduction information held by the reproduction information hold unit 2s7.

[0016]

Next, the header analysis unit 2s6 analyzes the header. When it becomes clear that the packet length is undefined, the data included in this packet is not audio or additional information data but video data. In this case, the controller 2s19 must perform as follows. That is, the controller 2s19 controls the switch SW1 so that the packet containing the video data is connected to the terminal c and, after the end of the header, transfers the coded video data area to the decoding buffer 2s9. On the other hand, the controller 2s19 connects the packet containing the video packet to the terminal b, and activates the start code prefix code detection unit 2s3 to detects the start code at the head of the next packet, and then detects the start code of the next packet to demultiplex the data of the next packet. However, there is a possibility that the hierarchy start code included in the hierarchically coded video sequence is confused with the packet start code because these codes have similar patterns and thereby the packet boundary is mistaken.

[0017]

Hereinafter, a description will be given of two examples of the case where the hierarchy start code of the coded video data

is divided between two packets, as patterns which are likely to mistake the packet boundary.

[0018]

Figure 4 shows examples of code sequence patterns which are likely mistake the packet boundary.

The packet boundary decision operation will be described for each of the patterns shown in figures 4(a) and 4(b).

Initially, the pattern of figure 4(a) will be described. In the pattern of figure 4(a), the hierarchy start code of the coded video data is divided into two packets, between '00' and ('00','01','00'). The start code prefix code detection unit 2s3 reads data from the input buffer 2s2 to detect the pattern of '00','00','01'. At this time, the read address of the input buffer 2s2 is address α. After detecting the pattern of '00','00','01', the start code prefix code detection unit 2s3 posts that it has detected the pattern, to the start code discrimination unit 2s5 in the subsequent stage, thereby activating the discriminating operation. Next, the start code discrimination unit 2s5 reads the data of address β, and decides whether this is an identifier indicating the head of the packet or a hierarchy start code of the coded video data.

[0019]

In the pattern of figure 4(a), since the data of address β is an identifier which indicates the start of the packet, the start code discrimination unit 2s5 posts that it has detected the

packet head, to the header analysis unit 2s6, thereby activating the header analysis unit 2s6. At this time, since the data of address γ is a portion of the coded video data, this data must be connected to the rear of the following video packet data and transferred to the decoding buffer 2s9. Therefore, before activating the header analysis unit 2s6, it is necessary to set the read address of the input buffer from address β to address γ which is prior to address β and, thereafter, transfer the data of address γ to the decoding buffer. Further, not only transferring the data of address α, it is necessary to store the information that the data of address α is a portion of the hierarchy start code of the coded video data.

[0020]

In the case of figure 4(b), after the start code discrimination unit 2s5 discriminates the identifier which indicates the packet start by address β, in order to transfer the data of addresses γ and δ which are parts of the coded video data to the decoding buffer 2s9, the read address of the input buffer which has been at address β should be returned to address γ to control transfer of the data of addresses γ and δ to the decoding buffer 2s9. Further, as in the case of figure 4(a), it is necessary to store the information that the data of addresses γ and δ are parts of the hierarchy start code of the coded video data.

[0021]

As described above, since the length of the video packet is undefined, the conventional coded and multiplexed signal reproduction apparatus performs complicated control, that is, not only advancing the reading pointer of the input buffer but also returning it at the packet boundary. To be specific, in the conventional apparatus, it is necessary to decide by the start code discrimination unit 2s5 as to whether or not the input packet is an elementary layer which is one layer lower than the video packet. However, data of a system layer is sometimes mixed into the video data and, in order to correct this, the data is successively transferred to the data separation control unit 2s8. At this time, the read pointer of the input buffer 2s2 must be returned by the input buffer read control circuit 2s4, and the input buffer read pointer correction unit 2s18 and the decoding buffer write pointer correction unit 2s17 are provided to perform the process of returning the pointer.

[0022]

That is, since data transfer and data discrimination are performed simultaneously in this conventional coded and multiplexed signal reproduction apparatus, writing must be performed with the write pointer advanced excessively to a position where the input data can be identified as data of the system layer. Hence, the write pointer of the decoding buffer 2s9 is advanced by using a decoding buffer write pointer correction unit 2s7. Further, when the input data is data of the

system layer, the start code must be detected again, and so the pointer value is once returned. In order to prevent the input data from being broken by this, an input buffer read pointer correction unit 2s18 is provided to correct the pointer of the input buffer 2s2. Further, in order to prevent the data input to the input buffer 2s2 from being broken, an input buffer protection unit 2s15 is provided to store the input data, whereby the input data is protected. Therefore, the construction and control of the apparatus are complicated.

[0023]

Secondary, in reproducing a coded and multiplexed signal, there is a case where header information of packets used for multiplexing must be used. As information required for this, audio and video synchronous reproduction information or the like is raised. In many cases, the reproduction information is given in fundamental units of audio and video reproduction. In the coded and multiplexed signal decoding apparatus, when the reproduction information is used for reproduction, it is necessary to store the information by any means. For example, it is thought that the reproduction information is temporarily stored in a memory or a register inside the coded and multiplexed signal decoding apparatus. However, when the reproduction information includes a lot of audio and video reproduction fundamental units in a unit time, hardware required as a memory or a register used for storage increases in size, resulting in

increased chip area when it is implemented by an LSI.

[0024]

Thirdly, when inputting coded and multiplexed data in the reproduction apparatus, confirmation as to whether a predetermined packet is input to the reproduction apparatus or not is sometimes important. In this case, the coded and multiplexed signal supply unit 2s1 should always monitor the number of data transmitted to the reproduction apparatus confirm that the last data of the packet is input to the reproduction apparatus, and this complicates the control of the coded and multiplexed signal supply unit 2s1.

[0025]

Fourthly, the reproduction apparatus for video and audio signals employs the pipeline structure in many cases. In the pipeline, a data bus width is defined, and coded data are transferred with the defined bus width to be decoded, but there occurs a case where the last part of the coded data is shorter than the data bus width. In order to control data transfer of the data shorter than the data bus width, it is necessary to perform data transfer control different from the ordinary data transfer in the pipeline, and this complicates the hardware.

[0026]

[Problems to be solved by the Invention]

As described above, in the patterns shown in figures 4(a) and 4(b), a complicated control circuit which performs control

such that the read address of the input buffer at the packet boundary is advanced and then returned back, is required, and this becomes a factor of increase in the hardware.

Further, many hardware resources, such as memories or registers, are used to retain the reproduction information included in the packet header section.

[0027]

The present invention is made to solve the above-mentioned problems of the conventional apparatus, and it is an object of the present invention to provide a coded and multiplexed signal reproduction apparatus which can reproduce a multiplexed digital signal without requiring complicated controls.

[0028]

[Measures to solve the Problems]

A coded and multiplexed signal reproduction apparatus according to the invention of Claim 1 comprises: a first multiplexed signal analysis unit for detecting a desired code sequence from code sequences in which data are multiplexed by using a synchronous signal and a packet length; a second multiplexed signal analysis unit for analyzing codes after the synchronous signal detected by the first multiplexed signal analysis unit, on the basis of synchronous signal establishment information generated by the first multiplexed signal analysis unit; a data separation control unit for recognizing the boundary of packets on the basis of synchronization establishment

information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit; and a formatter unit for generating data according to packet boundary information based on the synchronization establishment information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit, and inserting the data sequence in a predetermined position of separated data.

[0029]

Further, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 2 is a multiplexed video signal separation apparatus for separating a data sequence multiplexed by using a synchronous signal, a packet length, and packet header information including data reproduction information, comprising: a multiplexed signal analysis unit for analyzing a packet header; a data separation unit for performing desired data separation on the basis of the analysis result from the multiplexed signal analysis unit; and a formatter unit for inserting reproduction information obtained in the multiplexed signal analysis unit in a predetermined position of the separated data.

[0030]

Further, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 3 is an image signal reproduction apparatus comprising a coded and multiplexed signal separation unit having a pipeline structure and an image

signal decoding unit, wherein, when detecting a code sequence indicating the end of multiplexed data, the multiplexed signal separation unit adds padding data to the rear of the code sequence indicating the end of the multiplexed data.

[0031]

Further, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 4 is a coded and multiplexed signal reproduction apparatus having a pipeline structure wherein, when a signal of a specific data sequence is input, it is recognized as an input end of multiplexed data, and the pipeline is cleared.

[0032]

[Embodiments of the Invention]

Embodiment 1

Hereinafter, embodiments of the present invention will be described with reference to drawings. Figure 1 is a block diagram illustrating a coded and multiplexed signal reproduction apparatus according to a first embodiment of the present invention. This corresponds to the invention of Claim 1 of this application, providing simplified structure and control as compared with those of the conventional apparatus. The constituents of the apparatus having the same functions as those of the conventional apparatus are given the same reference numerals and, therefore, repeated description is not necessary.

[0033]

In figure 1, 2s14 is a start code prefix code detection status hold unit for receiving an output signal from the start code prefix code detection unit 2s3 and holding the status, and 2s13 is a formatter which receives an output signal from the header analysis unit 2s6, an output signal from the reproduction information hold unit 2s7, and an output signal from the start code prefix code detection status hold unit 2s14, and outputs a specific numerical sequence corresponding to an input numerical sequence according to these signals. The formatter generates data according to packet boundary information based on synchronization establishment information between the first multiplexed signal analysis unit and the second multiplexed signal analysis unit, and inserts the data sequence in a predetermined position of separated data. SW2 is a switch which selects one of the outputs from the start code prefix detection unit 2s3, the formatter 2s13, and the terminal c of the switch SW1, and outputs the selected signal. In this first embodiment, the input buffer protection unit 2s15, the start code status correction unit 2s16, the decoding buffer write pointer correction unit 2s17, the input buffer read pointer correction unit 2s18, and the switch SW3 are removed from the multiplexed signal separation unit 2s while the start code prefix code detection status hold unit 2s14 and the formatter 2s13 are added in the unit 2s.

[0034]

Next, the operation will be described. Description for parts which have already been described for the prior art and description for the case where an input packet is decided as an audio packet or an additional information packet, will be omitted. Hereinafter, only when an input packet is a video packet, especially the functions of the formatter 2s13 and the start code prefix code detection status hold unit 2s14 will be described with reference to the patterned of multiplexed data shown in figures 4(a) and 4(b).

[0035]

Under control of the controller 2s19, initially, the switch SW1 is connected to the contact b while the switch SW2 is connected to none of the contacts. The multiplexed data sequence stored in the input buffer 2s2 is output byte by byte toward the start code prefix code detection unit 2s3 under control of the input buffer reading control circuit 2s4. The start code prefix code detection unit 2s3 detects a packet start code which is a head code of packetized data, and activates the start code discrimination unit 2s5. The start code discrimination unit 2s5 decides the kind of the input packet by using that a video packet, an audio packet, and an additional information packet have different packet identifiers. When the packet identifier which follows the start code prefix code is an identifier which indicates a desired data sequence to be reproduced, the start code discrimination unit 2s5 posts that the input packet is an

effective packet to the header analysis unit 2s6. Whether the packet is an effective packet or an ineffective packet, the start code discrimination unit 2s5 activates the header analysis unit 2s6.

[0036]

When the start code discrimination unit 2s5 decides that the input packet is an audio packet, the controller 2s19 changes the connection of the switch SW1 from the contact b to the contact a, and outputs the video packet to the header analysis unit 2s6. At this time, the switch SW2 is connected to none of the contacts.

[0037]

On receipt of the packet from the input buffer 2s2, the header analysis unit 2s6 analyzes the packet length and the reproduction information used at reproduction, which are included in the packet header, and stores the reproduction information in the reproduction information hold unit 2s7. Further, the header analysis unit 2s6 decides the end of the header on the basis of the header information. While performing the processes of video data, the controller 2s19 controls the switch SW2 so that it is connected to none of the contacts, and activates the data separation control unit 2s8. The data separation control unit 2s8 controls data transfer to the decoding buffer 2s9 on the basis of the data separation information possessed by the header analysis unit 2s6.

[0038]

The coded data of video stored in the decoding buffer 2s9 is decoded by the video decoder in the decoding unit 2s10, like the coded data of audio or additional information, to be output as a reproduced signal. The decoding unit 2s10 performs the decoding process with the work memory 2s11. At this time, it performs the decoding operation so that the coded video data is synchronized with the coded audio data, by using the reproduction information held in the reproduction information hold unit 2s7.

[0039]

Next, the header analysis unit 2s6 performs analysis of the header. When it is confirmed that the data included in the input packet is video data, the controller 2s19 controls the switches SW1 and SW2 so that the packet containing this video data is connected to the terminals c and f, respectively. After the end of the header, the controller 2s19 connects the packet containing the video data through the terminal b of the switch SW1 to the start code prefix code detection unit 2s3 while transferring the coded video data area to the decoding buffer 2s9 side. Then, in order to detect the start code at the head of the next packet, the controller 2s19 activates the start code prefix code detection unit 2s3, and detects the next packet start code to separate the data of the next packet. However, there is a possibility that the hierarchy start code included in the hierarchically coded video sequence is confused with the packet start code because these codes have similar patterns, and thereby

the packet boundary is mistaken.

[0040]

Hereinafter, a description will be given of two examples in the case where the hierarchy start code of the coded video data is divided between two packets, as patterns of easily mistaking the packet boundary.

[0041]

First of all, the formatter 2s13 has a function of outputting one '00' in response to three numerical sequences '00' which are input thereto. The number of input '00' is known by referring to the output of the start code prefix code status hold unit 2s14 which is set by the start code prefix code detection unit 2s3.

[0042]

In the case of the pattern of figure 4(a), at the packet boundary, '00','00','00','01','E0' are input. Since a pattern of continuous three pieces of '00' is input, this status is detected by the start code prefix code detection unit 2s3 shown in figure 1, and this is stored in the start code prefix code detection status hold unit 2s14. When three pieces of '00' have been input continuously, the start code prefix code detection unit 2s3 activates the formatter 2s13. In response to this, the formatter 2s13 outputs one piece of '00' and, at this time, the controller 2s13 changes the connection of the switch SW2 from the terminal d to the terminal e, whereby this '00' is output through the

terminal e of the switch SW2 and the data separation control unit 2s8 to the decoding buffer 2s9. Thereby, the start code discrimination unit 2s5 decides that '00','00','00','01','E0' are packet codes. When this decision has been made, the '00' at the packet end is input to the decoding buffer 2s9. Since this '00' at the packet end is the head data of the hierarchy start code of the coded video data, this fact should be held. When the formatter 2s13 outputs one piece of '00' just before the start code discrimination unit 2s5 detects the packet start code, the status where one piece of '00' has been detected is set in the start code prefix code detection status hold unit 2s14 at the time when the start code discrimination unit 2s5 detects the packet start code. Therefore, it is not necessary to return back the data reading address of the input buffer 2s2 to read the data at the packet end.

[0043]

As described above, according to the first embodiment, since necessary data are generated by using the formatter, complicated control of advancing and backing the reading address of the input buffer is dispensed with when separating the coded and multiplexed signal. Therefore, control of the reading address of the input buffer by the input buffer reading control circuit is facilitated, and the hardware scale is reduced, thereby providing an apparatus for reproducing multiplexed digital code sequences, at a low price.

[0044]

Embodiment 2

Next, a second embodiment of the present invention will be described by using figure 1. This second embodiment 2 corresponds to Claim 2 of the present invention. In this second embodiment, it is not necessary to hold a lot of reproduction information in the apparatus and, therefore, hardware such as a memory or a register required for holding the reproduction information can be minimized.

[0045]

Figure illustrates a packet header of video and coded video data included in the packet header. It is assumed that head data is included in each reproduction fundamental unit of the coded video data. The reproduction information extracted by the header analysis unit 206 is temporarily stored in the reproduction information hold unit 2s7. As the reproduction information, display start information of each video reproduction fundamental unit is included in the packet. After analyzing the header section, the header analysis unit 2s6 activates the data separation control unit 2s8 to start transmission of vide data section toward the decoding buffer 2s9. At this time, in order to detect the boundary start code included in the coded video data, the start code prefix code detection unit 2s3, which is a multiplexed signal analysis unit performing analysis of the packet header, is activated. When the start code prefix code

detection unit 2s3 detects the start code prefix coded included in the video data, the start code prefix code detection unit 2s3 activates the start code discrimination unit 2s5 to decide whether the boundary start code of the video data is the start code of the reproduction fundamental unit or not. When the boundary start code of the video data is the start code of the separated data of the reproduction information obtained by the reproduction fundamental unit multiplexed signal analysis unit, the formatter 2s13, which is a formatter unit for inserting data in a predetermined position, adds the display start information as the reproduction information stored in the reproduction information hold unit 2s7 to the rear of the start code of the reproduction fundamental unit obtained by the data separation control unit 2s8 as a data separation unit for separating desired data on the basis of the analysis result from the multiplexed signal analysis unit.

[0046]

As described above, according to the second embodiment, since the formatter adds the reproduction information included in the packet header to the coded data of video, audio, and additional information, only the reproduction information included in the packet header is temporarily stored inside the reproduction apparatus. Therefore, it is not necessary to hold a lot of reproduction information in the apparatus, and the scale of hardware such as a memory or a register required for holding

the reproduction apparatus can be minimized, thereby providing an apparatus for reproducing multiplexed digital code sequences at a low price.

[0047]

Embodiment 3

Next, a third embodiment of the present invention will be described by using figure 1. This third embodiment corresponds to Claim 3 of the present invention. In this third embodiment, data are padded by using the formatter to simplify transfer control of a data bus through which data flow sequentially like a pipe line.

[0048]

Figure 6(a) illustrates a pattern of a code sequence at the rearmost portion of coded video data, in coded and multiplexed data. As is evident from figure 6(a), the rearmost portion of the coded video data has a data pattern which is shorter than the data width of a pipe line of the multiplexed signal separation unit 2s as a coded and multiplexed signal separation unit or the decoding unit 2s11 as an image signal decoding unit. The start code prefix code detection unit 2s3 detects a pattern of '00','00','01' from the input data pattern, and the start code discrimination unit 2s5 decides a boundary start code which indicates video end data. When the start code discrimination unit 2s5 detects the end part of the video end data, it posts this to the formatter 2s13. Then, the formatter 2s13 generates

video end data, and adds appropriate number of padding data 'FF' subsequently to the end data code sequence, and transfers these data to the decoding buffer 2s9. By adding the padding data, the video end data section which is shorter than the data bus width is aligned to the data bus width. At this time, as the padding data, it is necessary to select data which does not cause malfunction of the decoding unit, from data read from the decoding buffer 2s9. Then, the padding data is added to the end data sequence, whereby the code sequence including a code which is shorter than the data bus width of the pipeline required for decoding, can be transferred without necessity of complicated data bus transfer control.

[0049]

As described above, according to the third embodiment, the formatter has the data padding function to add the padding data at the rear of a specific code sequence. Therefore, data transfer in the pipeline inside the reproduction apparatus can be realized until the end portion of coded data which is shorter than the data bus width in the pipeline, without necessity of complicated transfer control. Thereby, reliable flow of the end portion of the coded data through the pipeline of the reproduction apparatus is realized without using complicated data transfer control.

[0050]

Embodiment 4.

Next, a fourth embodiment of the present invention will be described by using figure 1. This fourth embodiment corresponds to Claim 4 of the present invention. In this fourth embodiment, a unique code sequence is inserted in the last packet of the packet sequence in advance, whereby the host CPU can easily detect whether data are transmitted to the end or interrupted.

[0051]

Figure 7 shows a unique code sequence inserted in a packet boundary in a coded and multiplexed sequence. Assumed as a unique code sequence here is a code sequence similar to the packet start code. That is, the unique code sequence has a pattern like '00','00','01','XX'. However, selected as 'XX' is a code which is not confused with the packet start code. The host CPU 2s12 inserts the unique code sequence at the rear of specific packet data. When the unique code sequence is input to the rear of the specific data packet by the host CPU 2s12, the input of the unique code data is detected by the start code prefix code detection unit 2s3 and the start code discrimination unit 2s5 in the multiplexed signal separation unit 2s. At this time, the start code discrimination unit 2s5 posts that coded data included in a packet previous to the unique code sequence should be transferred to the decoding buffer 2s9, to the data separation control unit 2s8. On receipt of this, the data separation control unit 2s8 executes data transfer of the packet data to the decoding buffer 2s9, and when the transfer is completed, it posts

the completion of transfer to the start code discrimination unit 2s5. On receipt of this, the start code discrimination unit 2s5 posts that the unique code sequence is detected and the data included in the packet previous to the unique code sequence is transferred to the decoding buffer 2s9, to the host CPU 2s12. Thereby, the external host CPU 2s12 can reliably detect that the specific packet data is stored in the decoding buffer 2s9.

[0052]

As described above, according to the fourth embodiment, in the coded and multiplexed signal reproduction apparatus having the pipeline structure, when a specific data sequence signal is input, it is recognized as the input end of the multiplexed data, and the pipeline is cleared. When the last specific code sequence is input, data previous to the input specific code sequence is transferred to the decoding buffer and, thereafter, detection of the specific code sequence is posted to the external host CPU, whereby the external CPU can surely detect that data of a specific packet is input to the decoding buffer.

[0053]

While in the first to fourth embodiments a controller is provided besides the host CPU, the controller may be omitted by permitting the host CPU to have the function of controller as shown in figure 8, with the same effects as in the first to fourth embodiments.

[0054]

[Effects of the Invention]

As described above, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 1, comprises: a first multiplexed signal analysis unit for detecting a desired code sequence from code sequences in which data are multiplexed by using a synchronous signal and a packet length; a second multiplexed signal analysis unit for analyzing codes after the synchronous signal detected by the first multiplexed signal analysis unit, on the basis of synchronous signal establishment information generated by the first multiplexed signal analysis unit; a data separation control unit for recognizing the boundary of packets on the basis of synchronization establishment information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit; and a formatter unit for generating data according to packet boundary information based on the synchronization establishment information of both the first multiplexed signal analysis unit and the second multiplexed signal analysis unit, and inserting the data sequence in a predetermined position of separated data. Therefore, when separating a multiplexed signal, complicated control of reading addresses of the input buffer is dispensed with, and the scale of hardware is reduced, thereby providing an apparatus for reproducing multiplexed digital code sequences at a low price.

[0055]

Further, a coded and multiplexed signal reproduction

apparatus according to the invention of Claim 2 is a multiplexed video signal separation apparatus for separating a data sequence multiplexed by using a synchronous signal, a packet length, and packet header information including data reproduction information, comprising: a multiplexed signal analysis unit for analyzing a packet header; a data separation unit for performing desired data separation on the basis of the analysis result from the multiplexed signal analysis unit; and a formatter unit for inserting reproduction information obtained in the multiplexed signal analysis unit in a predetermined position of the separated data. Since the formatter adds the reproduction information included in the packet header to the coded data of video, audio, and additional information, the scale of hardware such as a memory or a register required for storage of the reproduction information can be reduced, thereby providing an apparatus for reproducing multiplexed digital code sequences at a low price.

[0056]

Further, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 3 is an image signal reproduction apparatus comprising a coded and multiplexed signal separation unit having a pipeline structure and an image signal decoding unit, wherein, when detecting a code sequence indicating the end of multiplexed data, the multiplexed signal separation unit adds padding data to the rear of the code sequence indicating the end of the multiplexed data. Therefore,

data transfer in the pipeline inside the reproduction apparatus can be performed until the end portion of coded data which is shorter than the data bus width of the pipeline, without necessity of complicated transfer control, thereby providing an apparatus for reproducing multiplexed digital code sequences at a low price.

[0057]

Further, a coded and multiplexed signal reproduction apparatus according to the invention of Claim 4 is a coded and multiplexed signal reproduction apparatus having a pipeline structure wherein, when a signal of a specific data sequence is input, it is recognized as an input end of multiplexed data, and the pipeline is cleared. Therefore, data transfer in the pipeline inside the reproduction apparatus can be performed until the end portion of coded data which is shorter than the data bus width of the pipeline, without necessity of complicated transfer control, thereby providing an apparatus for reproducing multiplexed digital code sequences at a low price.

[Brief Description of the Drawings]

[Fig.1] A block diagram illustrating a coded and multiplexed signal decoding apparatus according to first to fourth embodiments of the present invention.

[Fig.2] A block diagram illustrating a coded and multiplexed signal decoding apparatus according to the prior art.

[Fig.3] A diagram for explaining the structure of a

multiplexed signal.

[Fig.4] A diagram for explaining a multiplexed signal which is apt to mistake the packet boundary inside a decoding buffer.

[Fig.5] A diagram illustrating the relationship between a video packet and a fundamental unit of video reproduction.

[Fig.6] A diagram illustrating padding of a coded video data end portion by a formatter.

[Fig.7] A diagram illustrating a unique code sequence inserted in coded and multiplexed data.

[Fig.8] A block diagram illustrating a coded and multiplexed signal decoding apparatus according to first to fourth embodiments of the present invention.

[Description of Reference Numerals]

2 ... coded and multiplexed signal reproduction apparatus

2s ... multiplexed signal separation unit

2s1 ... coded and multiplexed data supply unit

2s2 ... input buffer

2s3 ... start code prefix code detection unit

2s4 ... input buffer reading control unit

2s5 ... start code discrimination unit

2s6 ... header analysis unit

2s7 ... reproduction information hold unit

2s8 ... data separation control unit

2s9 ... decoding buffer

2s10 ... decoding unit

2s11 ... work memory

2s12 ... host CPU

2s13 ... formatter

2s14 ... start code prefix code detector status hold unit

2s15 ... input buffer protection unit

2s16 ... start code status correction unit

2s17 ... decoding buffer write pointer correction unit

2s18 ... input buffer read pointer correction unit

2s19 ... controller

SW1 ... switch

SW2 ... switch

HB ... host bus

[Name of the Document] Abstract

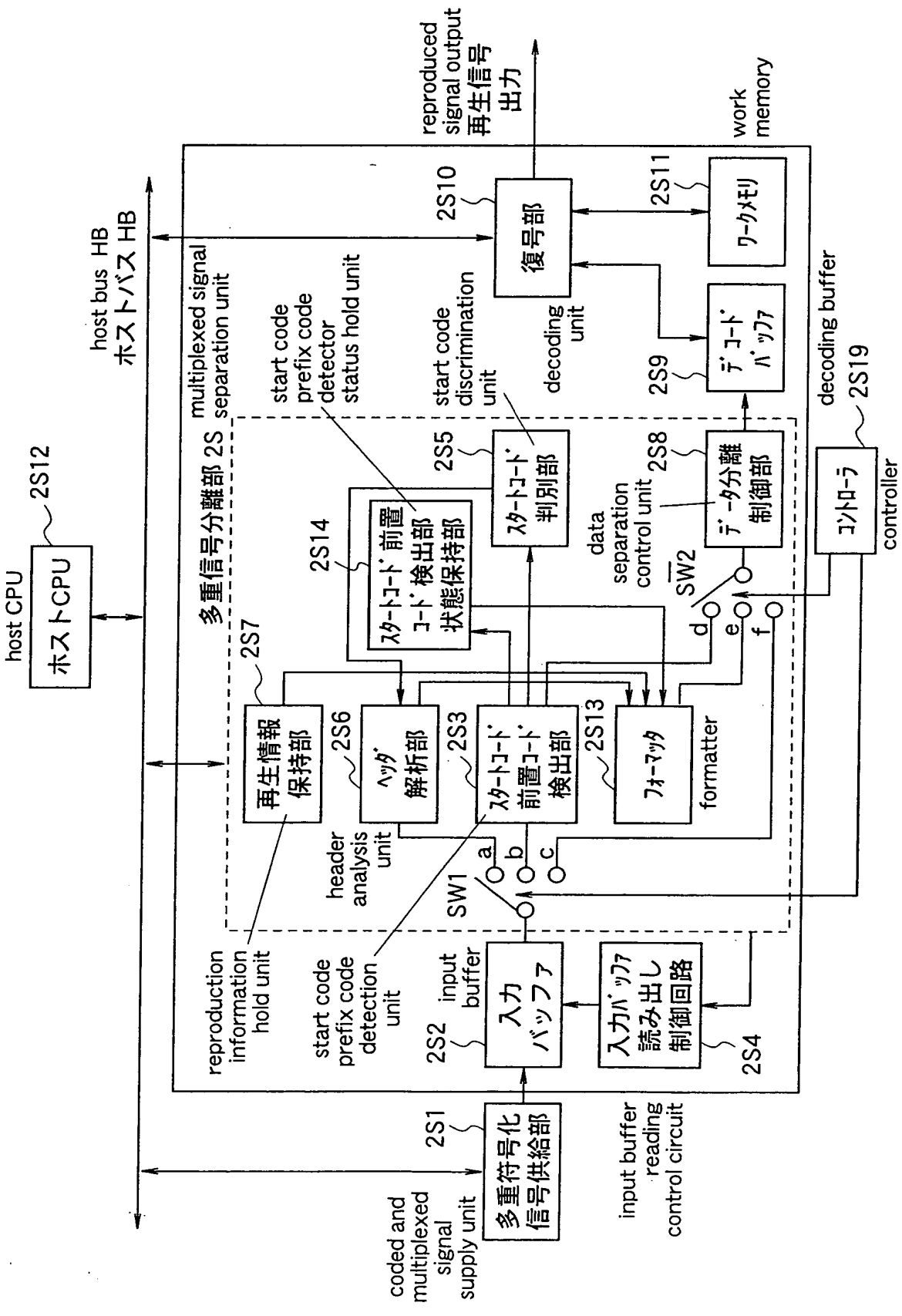
[Summary]

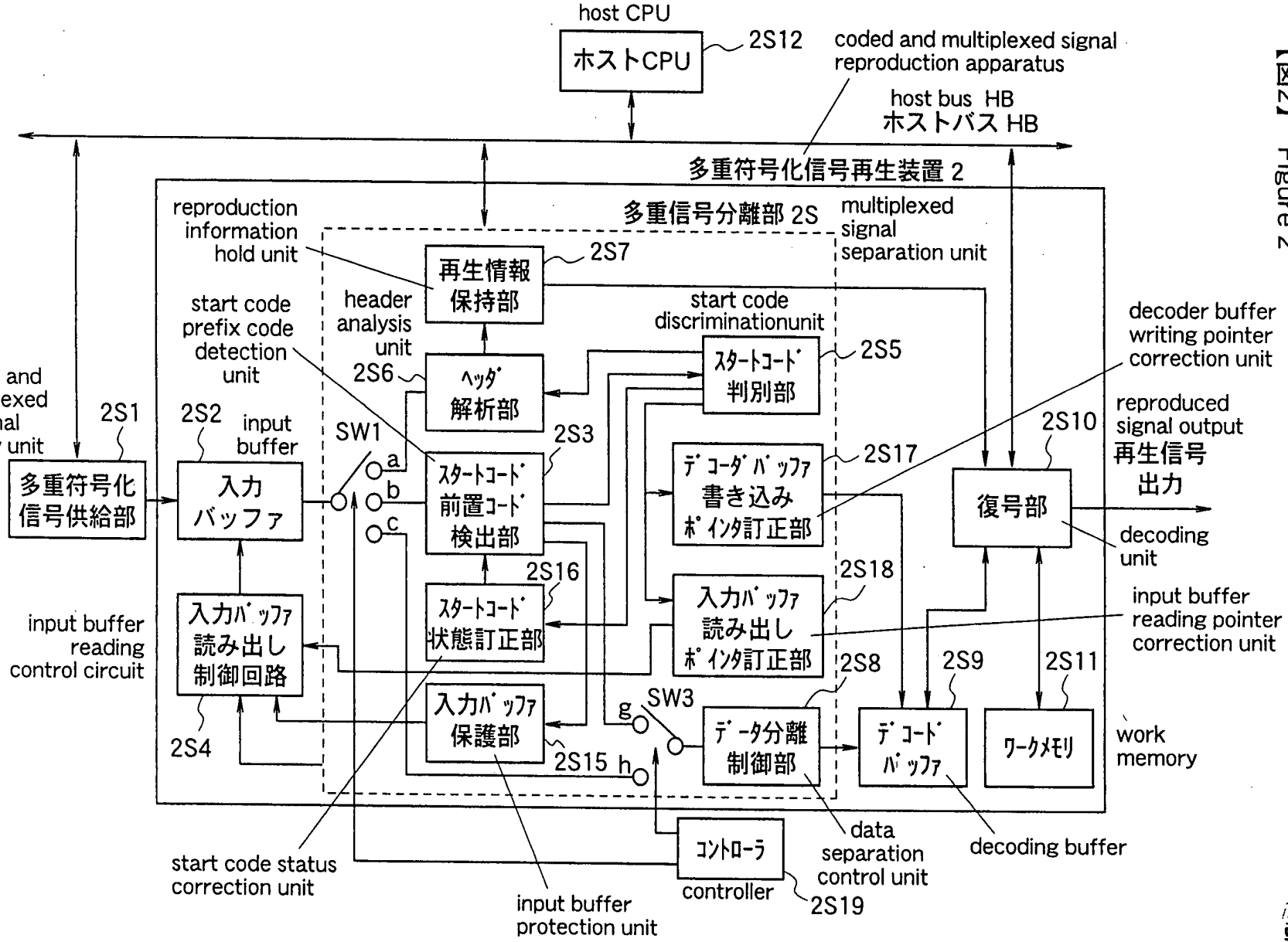
[Object] To simplify reading control of an input buffer in a multiplexed signal separation unit, in a coded and multiplexed signal separation and reproduction apparatus.

[Construction] A coded and multiplexed signal separation apparatus comprises a start code prefix code detection unit 2s3 for detecting a start code prefix code from a multiplexed code sequence in which data are multiplexed by using a synchronous signal and a packet length, and a header analysis unit 2s6 for analyzing codes after the synchronous signal detected by the start code prefix code detection unit 2s3. The apparatus further comprises a data separation control unit 2s8 for recognizing a packet boundary on the basis of information from both of the start code prefix code detection unit 2s3 and the header analysis unit 2s6, and a formatter 2s13 for generating data on the basis of packet boundary information from the data separation control unit 2s8, and inserting the data sequence in a predetermined position of separated data.

[Selected Figure] Figure 1

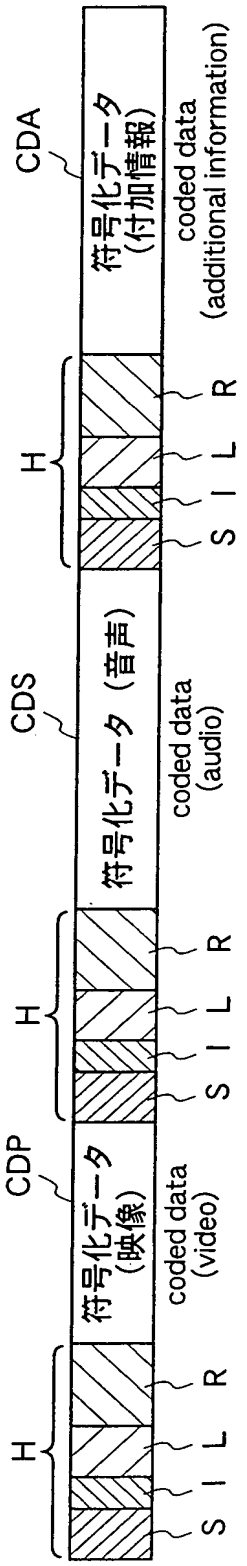
Name of Document
【書類名】　図面　Drawing
【図1】　Figure 1



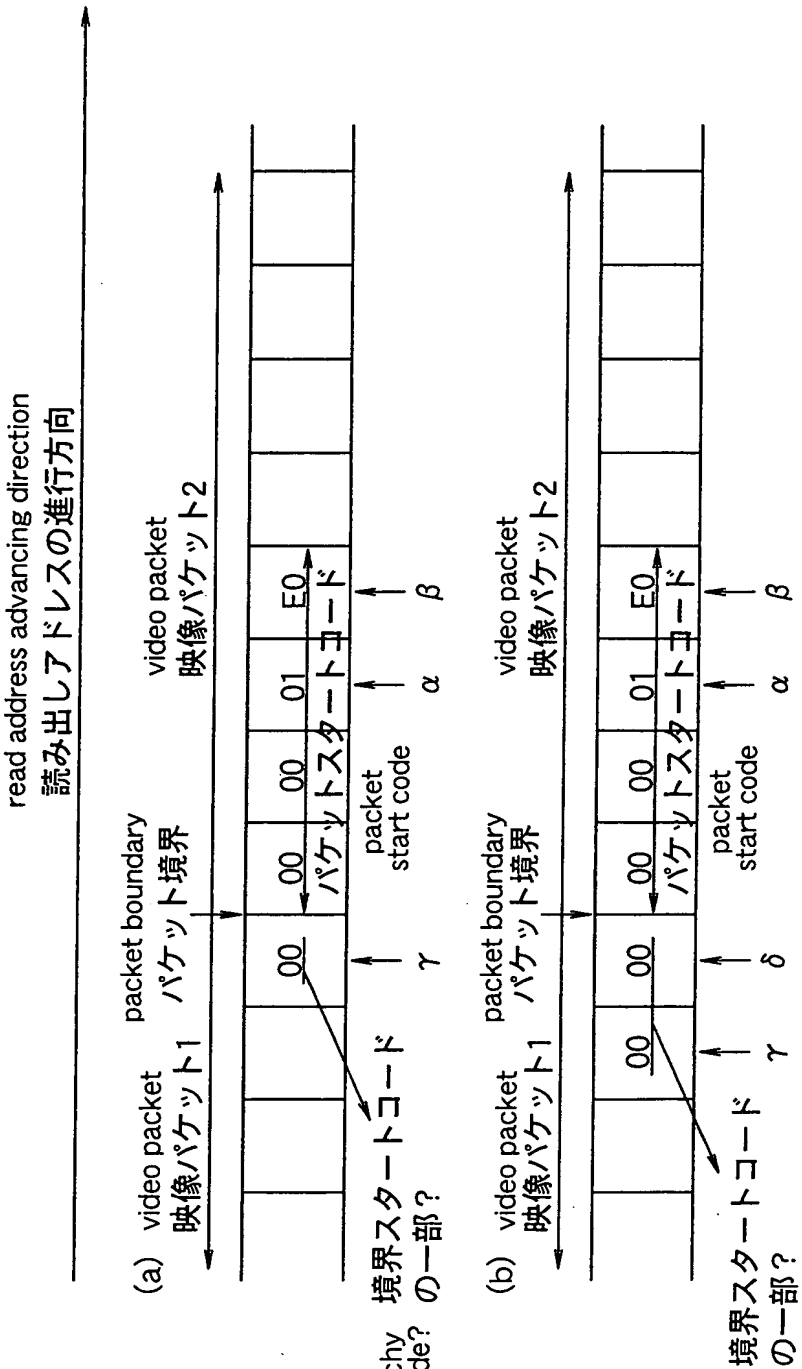


【図2】 Figure 2

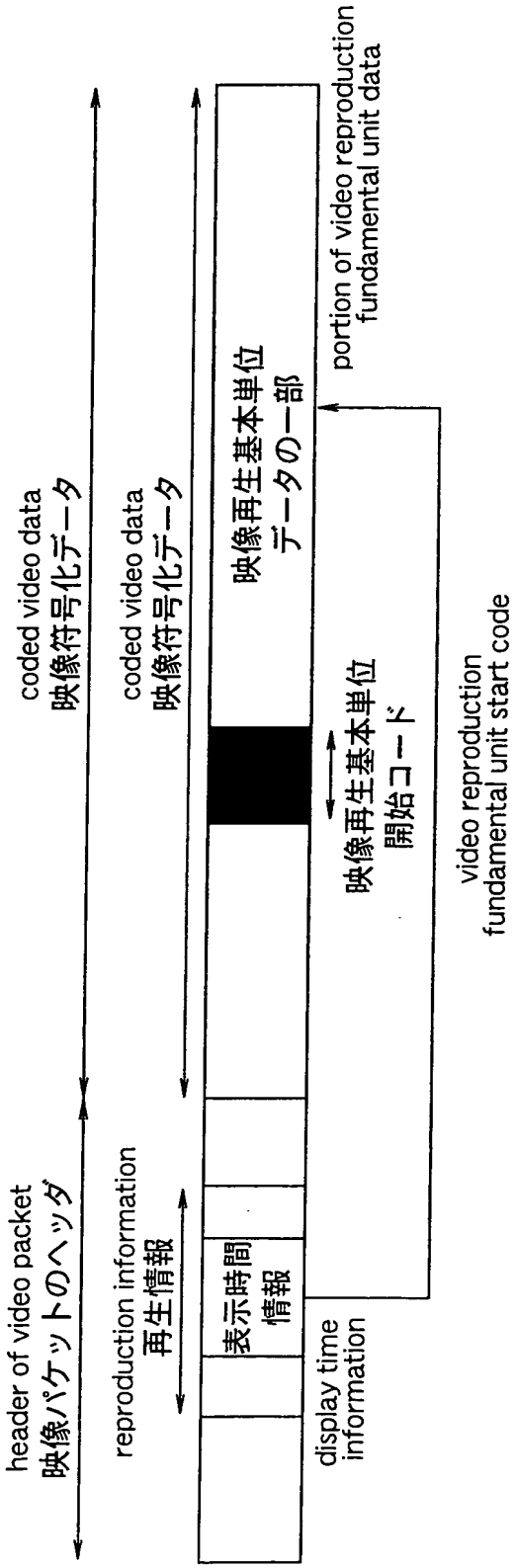
【図3】 Figure 3



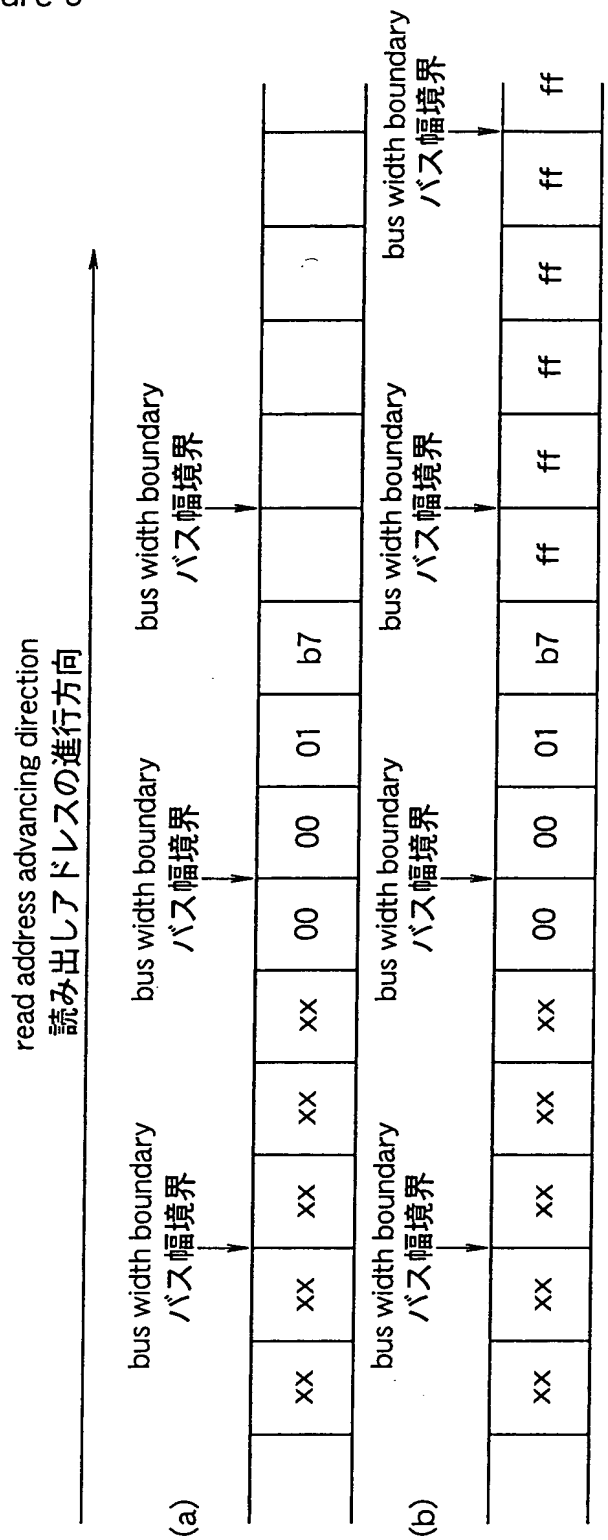
【図4】 Figure 4


read address advancing direction
読み出しアドレスの進行方向
(a) video packet
映像パケット1
packet boundary
パケット境界
video packet
映像パケット2
00
00
00
01
E0
パケットスタートコード
packet
start code
α
β
γ
境界スタートコード
の一部？
part of hierarchy
start code?
(b) video packet
映像パケット1
packet boundary
パケット境界
video packet
映像パケット2
00
00
00
01
E0
パケットスタートコード
packet
start code
α
β
γ
δ
境界スタートコード
の一部？
part of hierarchy
start code?

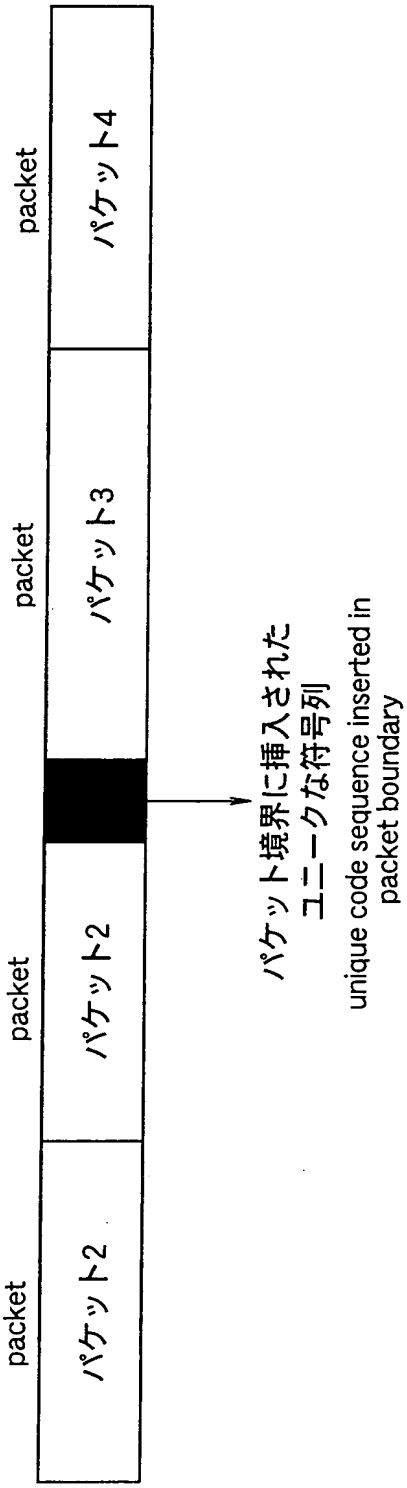
【図5】 Figure 5



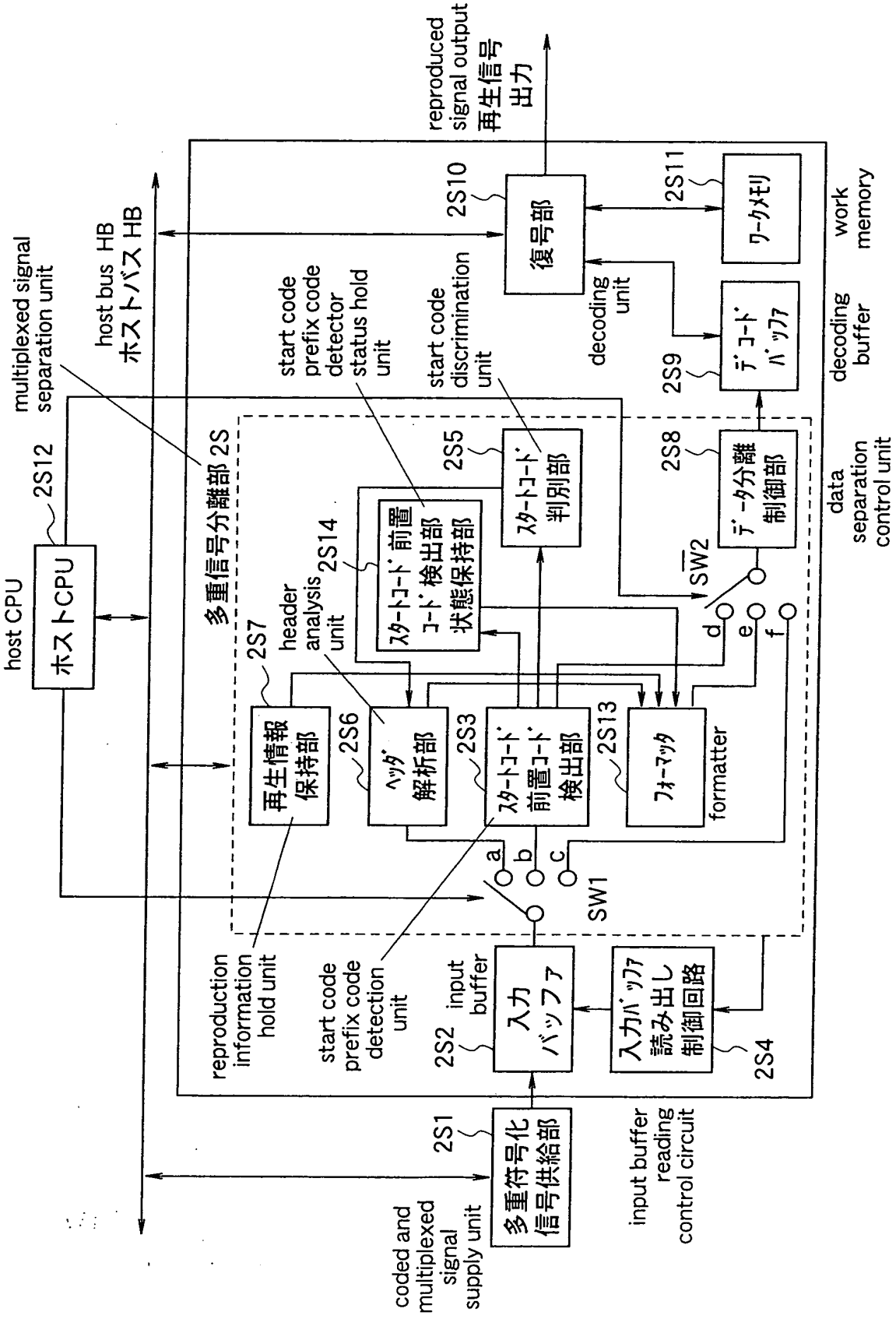
【図6】 Figure 6


read address advancing direction
読み出しアドレスの進行方向
(a)
(b)
bus width boundary
バス幅境界
xx
00
01
b7
ff

【図7】 Figure 7



【図8】 Figure 8


reproduced signal output
再生信号出力
host bus HB
ホストバス HB
multiplexed signal separation unit
host CPU
ホストCPU
2S12
多重信号分離部 2S
2S10
復号部
2S11
ワークメモリ
decoding unit
work memory
start code prefix code detector status hold unit
start code discrimination unit
2S9
デコードバッファ
decoding buffer
2S5
スタートコード判別部
2S8
データ分離制御部
data separation control unit
2S14
スタートコード前置コード検出状態保持部
header analysis unit
2S7
再生情報保持部
2S6
ヘッダ解析部
2S3
スタートコード前置コード検出部
2S13
フォーマッタ
formatter
SW2
SW1
a
b
c
d
e
f
reproduction information hold unit
start code prefix code detection unit
2S2
input buffer
入力バッファ
入力バッファ読み出し制御回路
2S4
2S1
多重符号化信号供給部
coded and multiplexed signal supply unit
input buffer reading control circuit